## AMENDMENTS TO THE CLAIMS

This listing of the claims replaces all prior versions, and listings, of claims in the application:

## LISTING OF CLAIMS

1. [Currently Amended] A carrier lock detector for use with a QPSK or low-level QAM system having a constellation of signal points identified by a plurality of I bits and Q bits respectively representing in-phase and quadrature components in a phasor diagram, the phasor diagram including a plurality of first areas centered on ideal signal points representing nominal states and a plurality of second areas adjacent to the first areas, the detector comprising:

   a first counter responsive to a plurality of I bits and Q bits, the first counter producing a first output signal when a detected signal has I and Q components that map a signal point onto one of the first areas;

   a second counter responsive to a plurality of I bits and Q bits, the second counter producing a second output signal when a detected signal has I and Q components that map a signal point onto one of the second areas; and

   a logic device for ~~computing a difference between the first output signal and the second output signal and for~~ generating a carrier lock detection signal ~~when the difference between the first output signal and the second output signal exceeds a threshold~~ using the first and second output signals~~.~~;

   wherein the first areas are defined by $(I_2 \oplus I_3) \cdot (Q_2 \oplus Q_3)$ and the second areas are defined by either one of $\overline{Q_1 \oplus Q_2} \cdot (I_1 \overline{I_2 I_3} + \overline{I_1} I_2 I_3) + (\overline{I_1 \oplus I_2}) \cdot (Q_1 \overline{Q_2 Q_3} + \overline{Q_1} Q_2 Q_3)$ and $(\overline{I_1 \oplus I_2} \cdot \overline{Q_2 \oplus Q_3}) + (\overline{Q_1 \oplus Q_2} \cdot \overline{I_2 \oplus I_3})$.

2. [Cancelled]

3. [Cancelled]

4. [Currently Amended] A coherent receiver with a carrier lock detector for use with a QPSK or low-level QAM system having a constellation of signal points identified by a plurality of I bits and Q bits respectively representing in-phase and quadrature components in a phasor diagram, the phasor diagram including a plurality of first areas centered on ideal signal points representing nominal states and a plurality of second areas adjacent to the first areas, comprising:

a first counter responsive to a plurality of I bits and Q bits, the first counter producing a first output signal when a detected signal has I and Q components that map a signal point onto one of the first areas;

a second counter responsive to a plurality of I bits and Q bits, the second counter producing a second output signal when a detected signal has I and Q components that map a signal point onto one of the second areas; and

a logic device for ~~computing a difference between the first output signal and the second output signal and for~~ generating a carrier lock detection signal ~~when the difference between the first output signal and the second output signal exceeds a threshold.~~ using the first and second output signals;

wherein the first areas are defined by $(I_2 \oplus I_3)\cdot(Q_2 \oplus Q_3)$ and the second areas are defined by either one of $\overline{Q_1 \oplus Q_2}\cdot\left(I_1\overline{I_2}\,\overline{I_3} + \overline{I_1}I_2I_3\right) + \left(\overline{I_1 \oplus I_2}\right)\cdot\left(Q_1\overline{Q_2}\,\overline{Q_3} + \overline{Q_1}Q_2Q_3\right)$ and $\left(\overline{I_1 \oplus I_2}\cdot\overline{Q_2 \oplus Q_3}\right) + \left(\overline{Q_1 \oplus Q_2}\cdot\overline{I_2 \oplus I_3}\right).$

5. [Original] The coherent receiver as claimed in claim 4, further comprising:

a local oscillator for generating a local signal having a local frequency different from that of a received signal;

a coupler for combining the incoming signal with the local signal to produce an intermediate signal;

a detector for detecting the intermediate signal;

a filter for filtering the intermediate signal;

a demodulator for separating the intermediate signal into analog I and Q components;

a first analog-to-digital converter for converting the analog I components into I bits; and

a second analog-to-digital converter for converting the analog Q components into Q bits.

6. [Original] The coherent receiver as claimed in claim 5 wherein the first analog-to-digital converter is a 3-bit analog-to-digital converter for decoding I bits designated as $I_1$, $I_2$, $I_3$ where $I_1$ is the most significant I bit; and the second analog-to-digital converter is a 3-bit analog-to-digital converter for decoding Q bits designated as $Q_1$, $Q_2$, $Q_3$, where $Q_1$ is the most significant Q bit.

7. [Cancelled]

8. [Cancelled]

9. [Currently Amended] The coherent receiver as claimed in claim ~~7~~ 5 wherein the local oscillator comprises a laser.

10. [Currently Amended] The coherent receiver as claimed in claim ~~9~~ 5 wherein the detector comprises a photodiode.

11. [Currently Amended] The coherent receiver as claimed in claim ~~10~~ 5 wherein the filter comprises a low-pass filter ~~and an AC coupling~~.

12. [Currently Amended] The coherent receiver as claimed in claim ~~11~~ 5 wherein the coupler is an optical hybrid.

13. [Cancelled]

14. [Cancelled]

15. [Cancelled]

16. [Cancelled]

17. [Currently Amended] A method of detecting carrier lock in a QPSK or low-level QAM system having a constellation of signal points identified by a plurality of I bits and Q bits respectively representing in-phase and quadrature components in a phasor diagram, the phasor diagram including a plurality of first areas centered on ideal signal points representing nominal states and a plurality of second areas adjacent to the first areas, the method comprising the steps of:

monitoring a plurality of less significant I and Q bits;

generating a first signal when a detected received signal has I and Q components that map onto one of the first areas;

generating a second signal when the detected received signal has I and Q components that map onto one of the second areas; and

~~computing a difference between the first signal and the second signal;~~

~~comparing the difference with a threshold value; and~~

generating a carrier lock detection signal ~~when the difference exceeds the threshold.~~based on the first and second signals;

wherein the first areas are defined by $(I_2 \oplus I_3)\cdot(Q_2 \oplus Q_3)$ and the second areas are defined by either one of $\overline{Q_1 \oplus Q_2}\cdot\left(I_1\overline{I_2 I_3}+\overline{I_1}I_2I_3\right)+\left(\overline{I_1 \oplus I_2}\right)\cdot\left(Q_1\overline{Q_2Q_3}+\overline{Q_1}Q_2Q_3\right)$ and $\left(\overline{I_1 \oplus I_2}\cdot\overline{Q_2 \oplus Q_3}\right)+\left(\overline{Q_1 \oplus Q_2}\cdot\overline{I_2 \oplus I_3}\right)$.

18. [Cancelled]

19. [Cancelled]

20. [Cancelled]

21. [NEW] The carrier lock detector as claimed in claim 1, wherein the logic device comprises:

a first digital filter connected to receive the first output signal, for generating a respective first average signal P1 indicative of a probability that the detected signals map onto one of the first areas;

a second digital filter connected to receive the second output signal, for generating a respective second average signal P2 indicative of a probability that the detected signals map onto one of the second areas;

a digital adder/subtractor for computing a difference between the first and second average signals; and

a threshold comparator for comparing the subtraction result to a predetermined threshold, and for generating the carrier lock detection signal based on the comparison result.

22. [NEW] The carrier lock detector as claimed in claim 21, wherein each of the first and second average signals P1 and P2 is a running average computed over a predetermined number of samples of the first and second output signals, respectively.

23. [NEW] The coherent receiver as claimed in claim 4, wherein the logic device comprises:

a first digital filter connected to receive the first output signal, for generating a respective first average signal P1 indicative of a probability that the detected signals map onto one of the first areas;

a second digital filter connected to receive the second output signal, for generating a respective second average signal P2 indicative of a probability that the detected signals map onto one of the second areas;

a digital adder/subtractor for computing a difference between the first and second average signals; and

a threshold comparator for comparing the subtraction result to a predetermined threshold, and for generating the carrier lock detection signal based on the comparison result.

24. [NEW] The coherent receiver as claimed in claim 23, wherein each of the first and second average signals P1 and P2 is a running average computed over a predetermined number of samples of the first and second output signals, respectively.

25. [NEW] The method as claimed in claim 17, wherein the step of generating the carrier lock detection signal comprises steps of:

computing a first average signal P1 indicative of a probability that the detected signals map onto one of the first areas;

computing a second average signal P2 indicative of a probability that the detected signals map onto one of the second areas

computing a difference between the first and second average signals;

comparing the difference with a threshold value; and

generating the carrier lock detection signal based on the detection result.

26. [NEW] The method as claimed in claim 24, wherein the steps of computing the first and second average signals P1 and P2 comprise computing respective running averages over a predetermined number of symbols of the first and second output signals, respectively.